

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Patrick J. Garavan  
Serial No: --  
Confirmation No: --  
Filed: April 13, 2004  
For: SWITCHED BANDGAP REFERENCE CIRCUIT  
  
Examiner: --  
Art Unit: --

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

STATEMENT FILED PURSUANT TO THE DUTY OF  
DISCLOSURE UNDER 37 CFR §§1.56, 1.97 AND 1.98

Sir:

Pursuant to the duty of disclosure under 37 C.F.R. §§1.56, 1.97 and 1.98, the Applicant requests consideration of this Information Disclosure Statement.

PART I: Compliance with 37 C.F.R. §1.97

☒ This Information Disclosure Statement has been filed before the mailing date of a first Office Action on the merits in the above-identified case.

No fee or certification is required.

PART II: Information Cited

☒ The Applicant hereby makes of record in the above-identified application the information listed on the attached form PTO-1449 (modified). The order of presentation of the references should not be construed as an indication of the importance of the references.

Part III: Remarks

Documents cited anywhere in the Information Disclosure Statement are enclosed unless otherwise indicated. It is respectfully requested that:

1. The Examiner consider completely the cited information, along with any other information, in reaching a determination concerning the patentability of the present claims;

2. The enclosed form PTO-1449 be signed by the Examiner to evidence that the cited information has been fully considered by the Patent and Trademark Office during the examination of this application;

3. The citations for the information be printed on any patent which issues from this application.

By submitting this Information Disclosure Statement, the Applicant makes no representation that a search has been performed, of the extent of any search performed, or that more relevant information does not exist.


By submitting this Information Disclosure Statement, the Applicant makes no representation that the information cited in the Statement is, or is considered to be, material to patentability as defined in 37 C.F.R. §1.56(b).

By submitting this Information Disclosure Statement, the Applicant makes no representation that the information cited in the Statement is, or is considered to be, in fact, prior art as defined by 35 U.S.C. §102.

Notwithstanding any statements by the Applicant, the Examiner is urged to form his own conclusion regarding the relevance of the cited information.

An early and favorable action is hereby requested.

Respectfully submitted,  
Patrick J. Garavan, *Applicant*

By:   
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Docket No. H0682.70006 US00  
Date: April 13, 2004  
**XNDDX**

<b>FORM PTO-1449/A and B (Modified)</b>  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>				APPLICATION NO.: --		ATTY. DOCKET NO.: H0682.70006 US00	
				FILING DATE: April 13, 2004		CONFIRMATION NO.: --	
				APPLICANT: Patrick J. Garavan			
				GROUP ART UNIT: --		EXAMINER: --	
Sheet	1	of	1				

#### U.S. PATENT DOCUMENTS

Examiner's Initials	Cite No.	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication or of issue of Cited Document MM-DD-YYYY
		Number	Kind Code		
		5,059,820		Westwick	10-22-1991
		5,352,973		Audy	10-04-1994
		5,867,012		Tuthill	02-02-1999

#### FOREIGN PATENT DOCUMENTS

Examiner's Initials	Cite No.	Foreign Patent Document			Name of Patentee or Applicant of Cited Document (not necessary)	Date of Publication of Cited Document MM-DD-YYYY	Translation (Y/N)
		Office/ Country	Number	Kind Code			

#### OTHER ART — NON PATENT LITERATURE DOCUMENTS

Examiner's Initials	Cite No	Include name of the author (in CAPITAL LETTERS) title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, relevant page(s), volume-issue number(s), publisher, city and/or country where published.	Translation (Y/N)	
		Meijer, G.C.M., et al, "A New Curvature-Corrected Bandgap Reference", IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 6, Dec 1982.		
		Razavi, B., "CMOS Processing Technology", Chap. 17 - <u>Design of Analog CMOS Integrated Circuits</u> , McGraw Hill, International Edition 2001.		

EXAMINER	DATE CONSIDERED
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#EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

\*a copy of this reference is not provided as it was previously cited by or submitted to the office in a prior application, Serial No. \_\_, filed \_\_, and relied upon for an earlier filing date under 35 U.S.C. 120 (continuation, continuation-in-part, and divisional applications).

[NOTE - Must provide a copy of any patent, publication, other information listed, even if it was previously submitted to, or cited by, the U.S. Patent Office in an earlier application, unless the earlier application is identified by the IDS and is relied upon for an earlier filing date under 35 U.S.C. §120, and the copy was provided in the earlier application.]